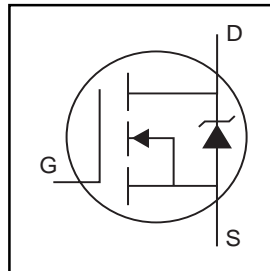


- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching

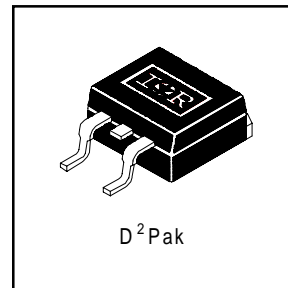
Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters in the PC environment. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



$V_{DSS} = 20V$
$R_{DS(on)} = 0.016\Omega$
$I_D = 48A$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ Ⓞ	48	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ Ⓞ	30	
I_{DM}	Pulsed Drain Current ①Ⓞ	190	
$P_D @ T_C = 25^\circ C$	Power Dissipation	69	W
	Linear Derating Factor	0.56	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
V_{GSM}	Gate-to-Source Voltage (Start Up Transient, $t_p = 100\mu s$)	14	V
E_{AS}	Single Pulse Avalanche EnergyⓄⓄ	270	mJ
I_{AR}	Avalanche Current①	29	A
E_{AR}	Repetitive Avalanche Energy①	6.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③Ⓞ	5.0	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 150	°C
T_{STG}			

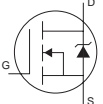
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.8	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V _{GS} = 0V, I _D = 250μA
dV _{(BR)DSS} /dT _J	Breakdown Voltage Temp. Coefficient	—	0.029	—	V/°C	Reference to 25°C, I _D = 1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.019	mΩ	V _{GS} = 4.5V, I _D = 29A ^④
		—	—	0.016		V _{GS} = 7.0V, I _D = 29A ^④
V _{GS(th)}	Gate Threshold Voltage	0.70	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	28	—	—	S	V _{DS} = 16V, I _D = 29A ^⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 20V, V _{GS} = 0V
		—	—	250		V _{DS} = 10V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 10V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -10V
Q _g	Total Gate Charge	—	—	43	nC	I _D = 29A
Q _{gs}	Gate-to-Source Charge	—	—	12		V _{DS} = 16V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	13		V _{GS} = 4.5V, See Fig. 6 ^{④⑤}
t _{d(on)}	Turn-On Delay Time	—	9.8	—	ns	V _{DD} = 10V
t _r	Rise Time	—	100	—		I _D = 29A
t _{d(off)}	Turn-Off Delay Time	—	63	—		R _G = 9.5mΩ, V _{GS} = 4.5V
t _f	Fall Time	—	82	—		R _D = 0.3mΩ, ^{④⑤}
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	2000	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	800	—		V _{DS} = 15V
C _{rss}	Reverse Transfer Capacitance	—	290	—		f = 1.0MHz, See Fig. 5 ^⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	48	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^{①⑤}	—	—	190		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 29A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	68	100	ns	T _J = 25°C, I _F = 29A
Q _{rr}	Reverse Recovery Charge	—	130	190	nC	di/dt = 100A/μs ^{④⑤}
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.64mH
R_G = 25mΩ, I_{AS} = 29A.

③ I_{SD} ≤ 29A, di/dt ≤ 63A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 150°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRL3202 data and test conditions

** When mounted on FR-4 board using minimum recommended footprint.

For recommended footprint and soldering techniques refer to application note #AN-994.

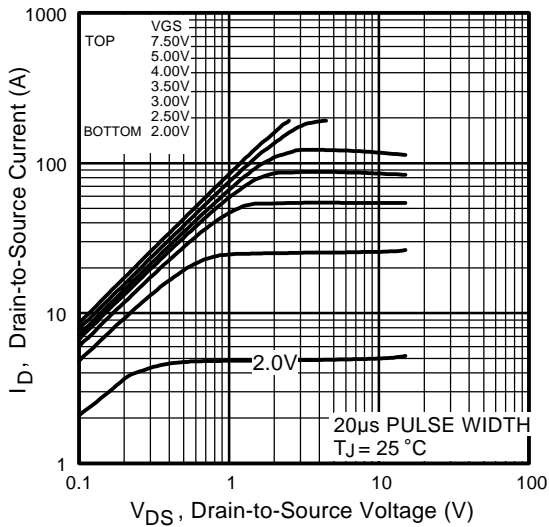


Fig 1. Typical Output Characteristics

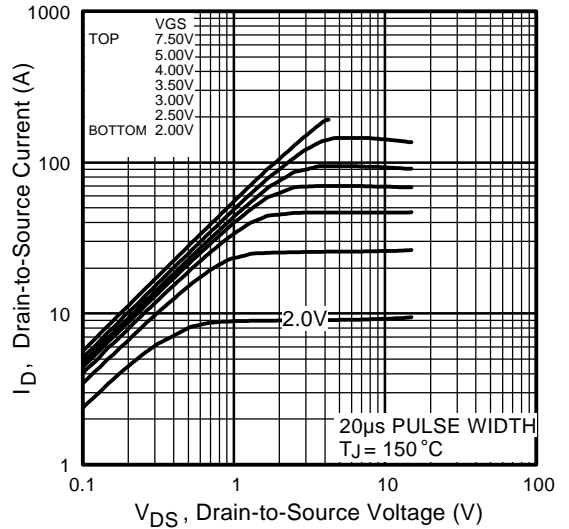


Fig 2. Typical Output Characteristics

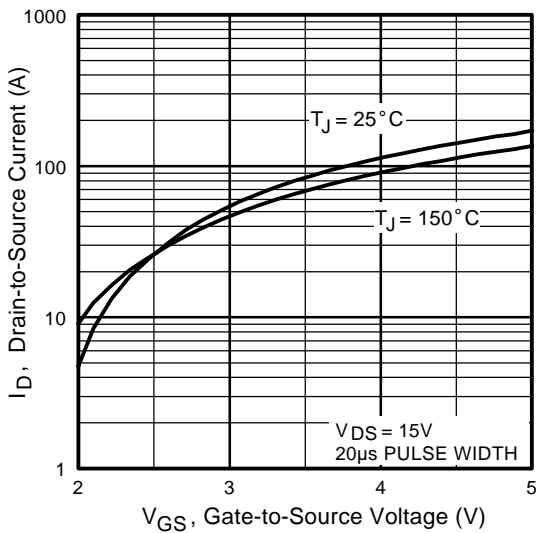


Fig 3. Typical Transfer Characteristics

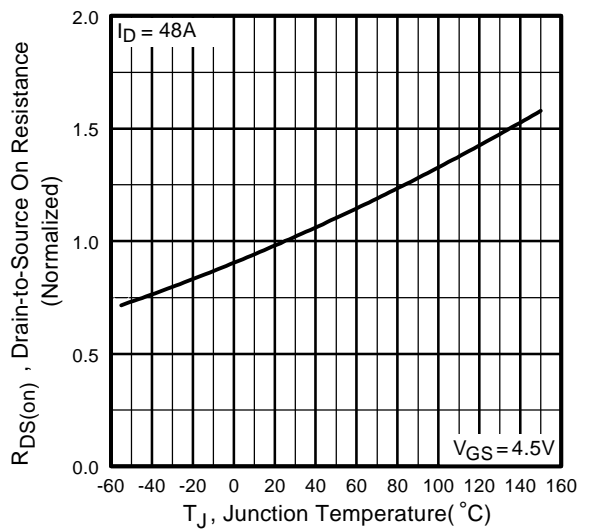


Fig 4. Normalized On-Resistance Vs. Temperature

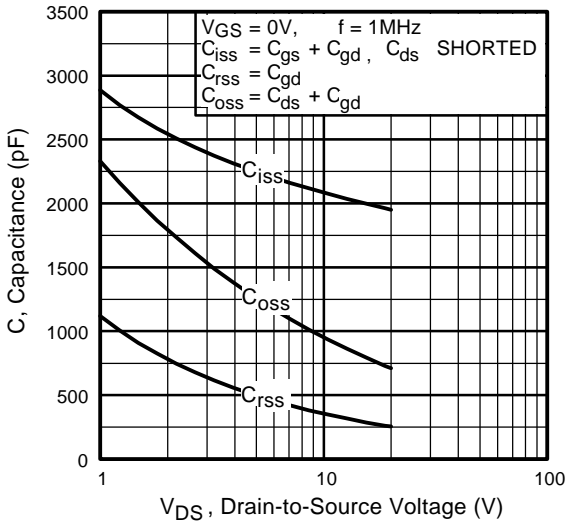


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

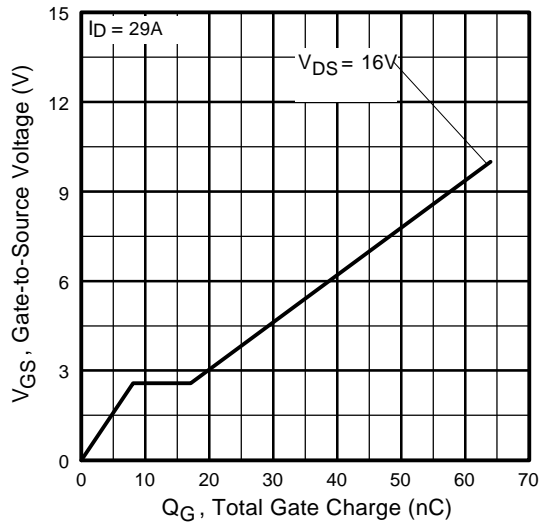


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

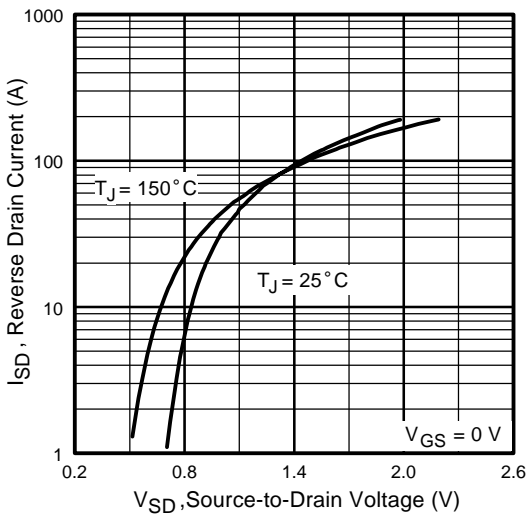


Fig 7. Typical Source-Drain Diode Forward Voltage

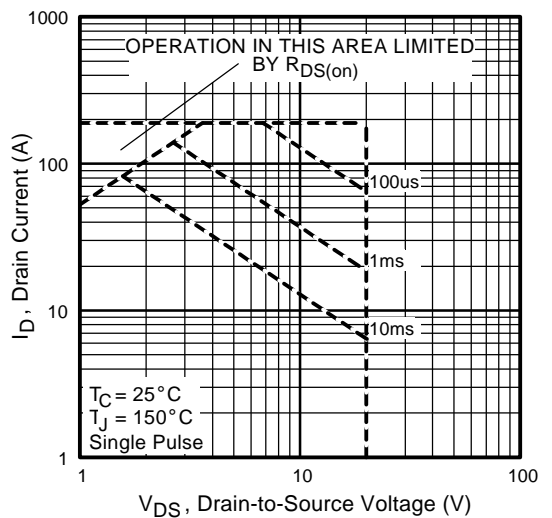


Fig 8. Maximum Safe Operating Area

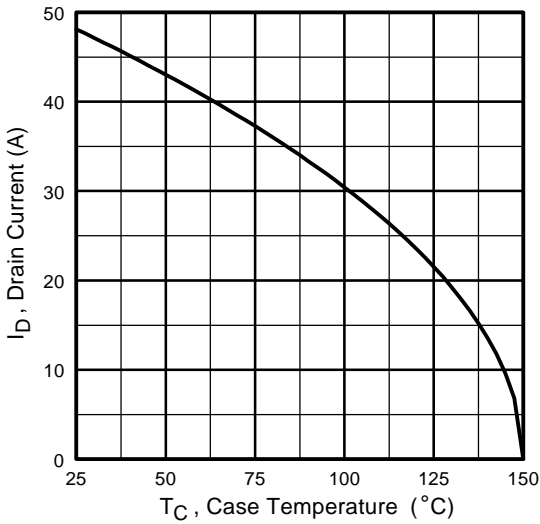


Fig 9. Maximum Drain Current Vs. Case Temperature

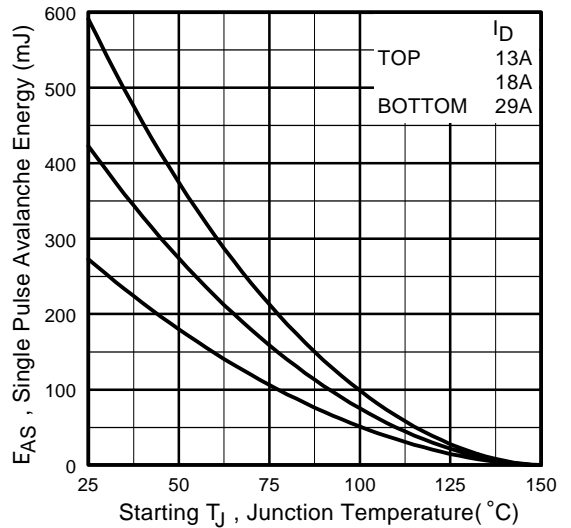


Fig 10. Maximum Avalanche Energy Vs. Drain Current

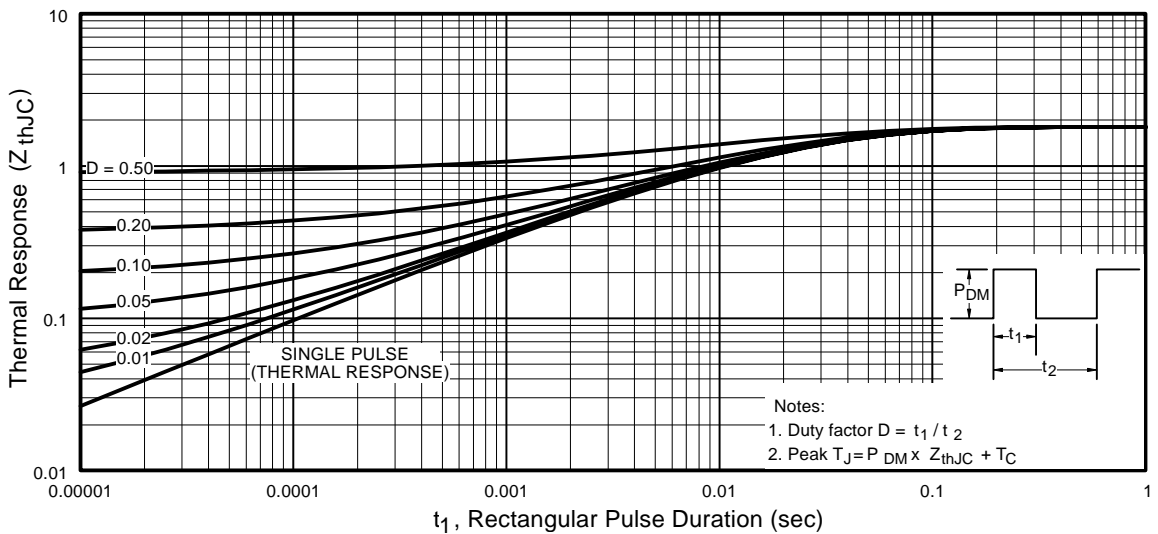


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

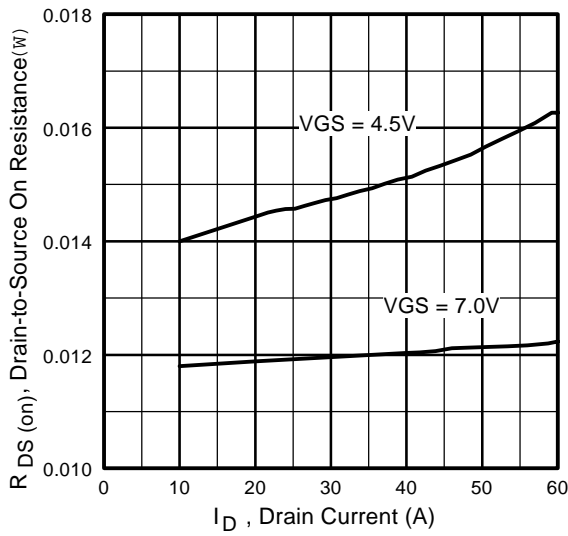


Fig 12. On-Resistance Vs. Drain Current

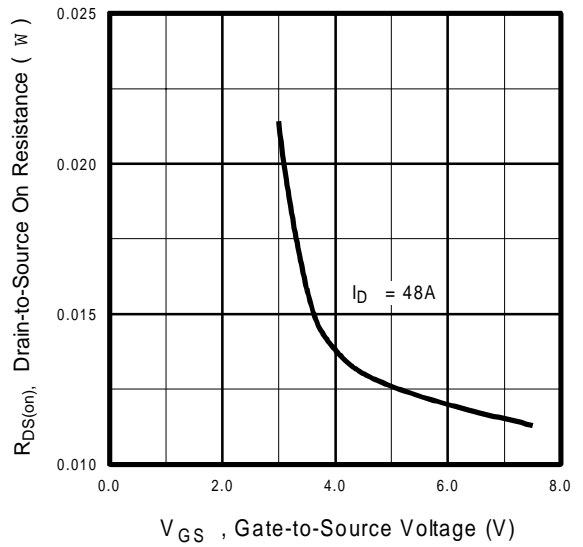
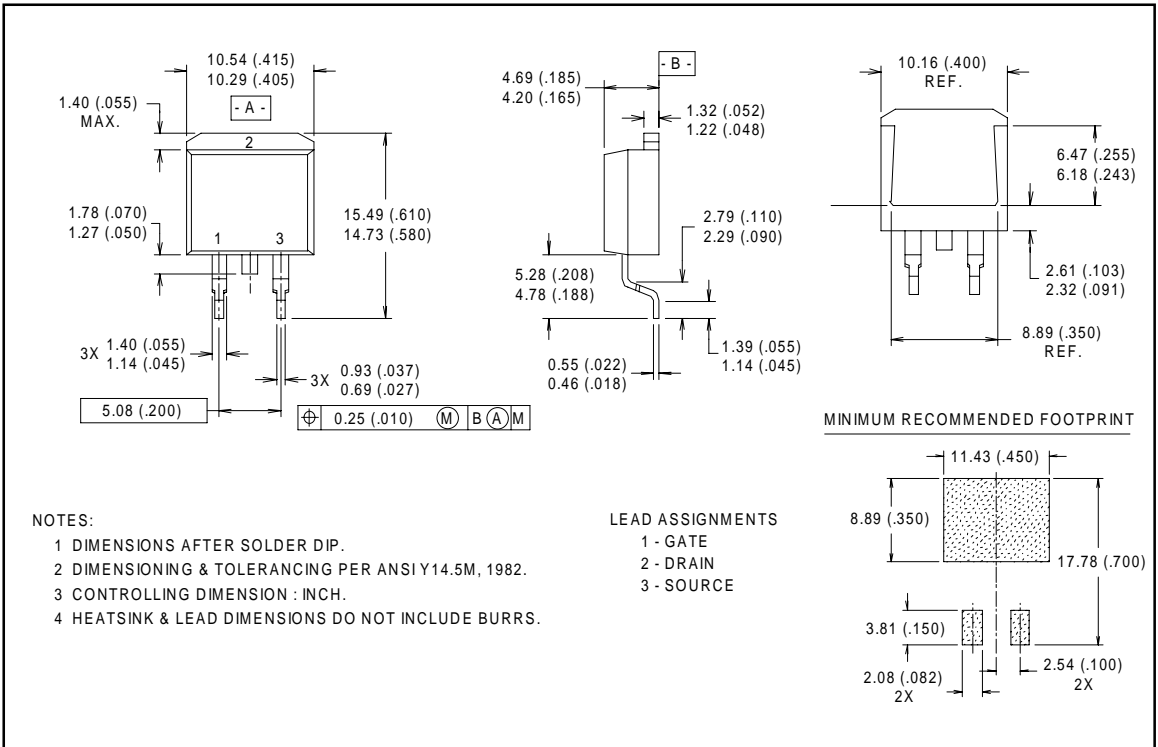


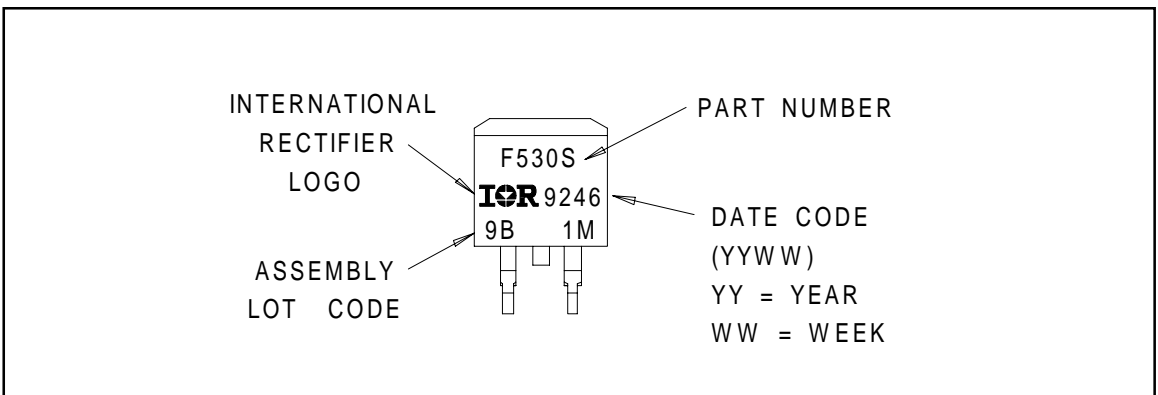
Fig 13. On-Resistance Vs. Gate Voltage

D²Pak Package Outline



Part Marking Information

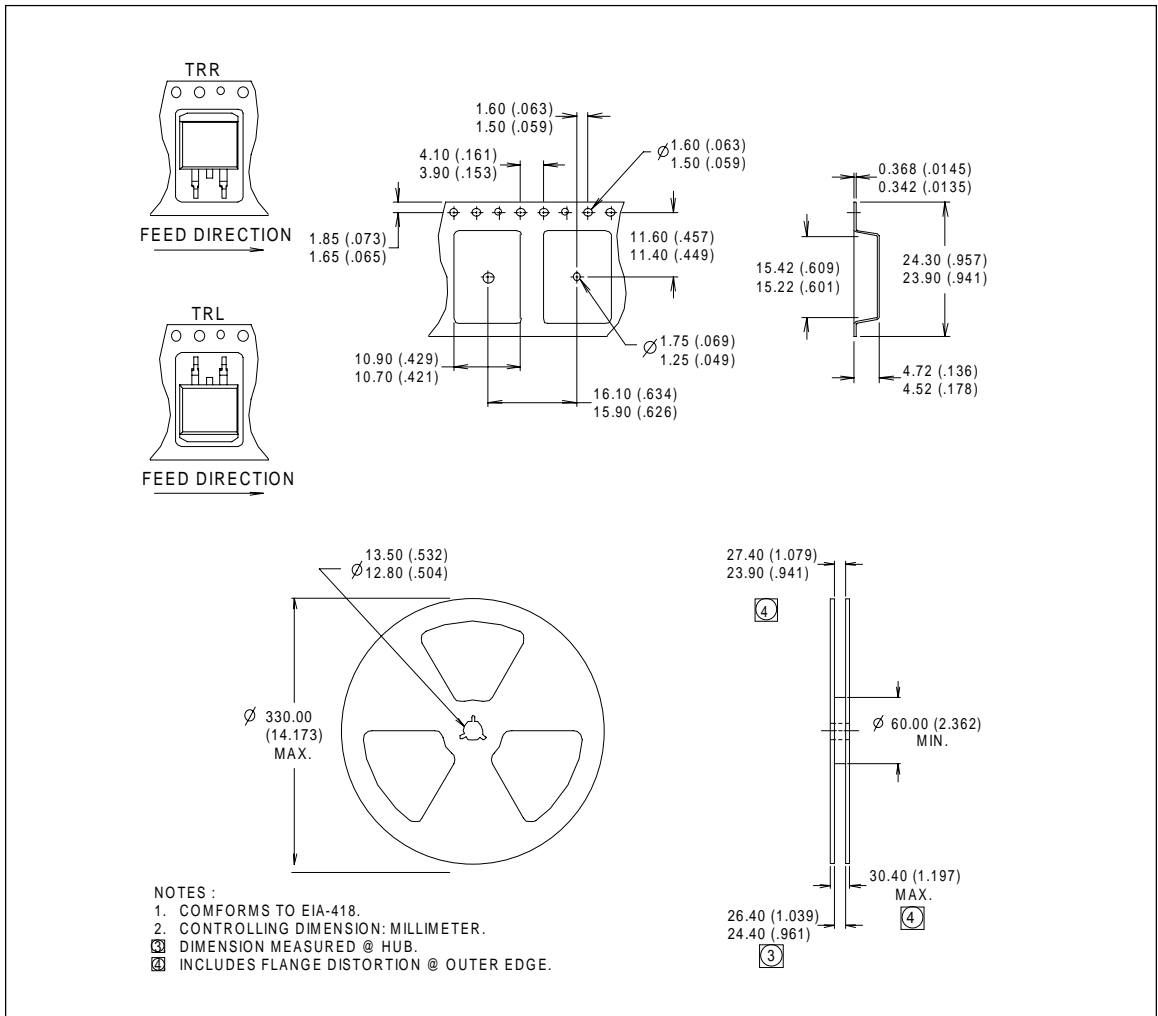
D²Pak



IRL3202S

Tape & Reel Information

D²Pak



WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>